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LIMA

劉 成  
Sales Engineer  
S.Z.Mobile:136-8239-6505  
MSN:szlima@hotmail.com  
QQ:778174600

AVAGO 光耦一级代理商

利瑪電子(新加坡)有限公司  
Add:深圳市華強北電子科技大廈A座3908室  
Tel:0755-8250 8350 Fax:0755-8836 4656  
E-mail:lima@limaic.com  
Website:www.limaic.com

Optocoupler  
World



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Current Revision 1.0

HISTORY

NO.1    AUTHOR        : [张志晨]  
         DATA        : [2008-05-10]  
         VERSION     : [1.0 (beta)]  
         DESTINATION: [creation]  
         NOTE: []



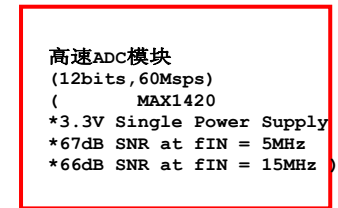
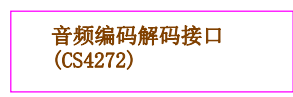
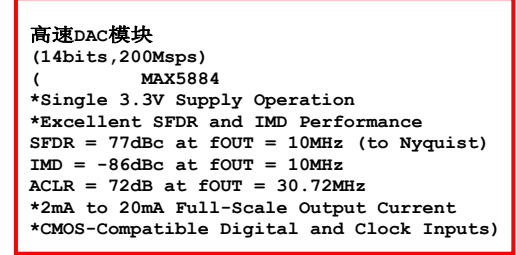
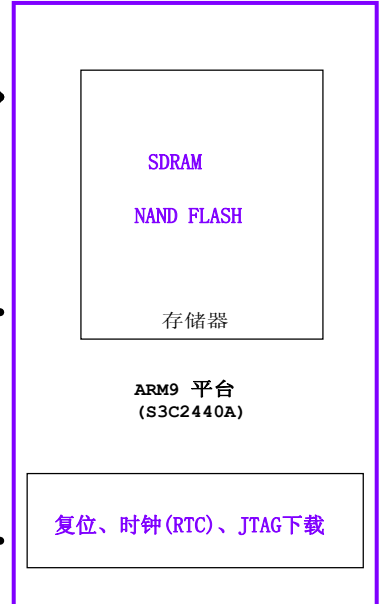
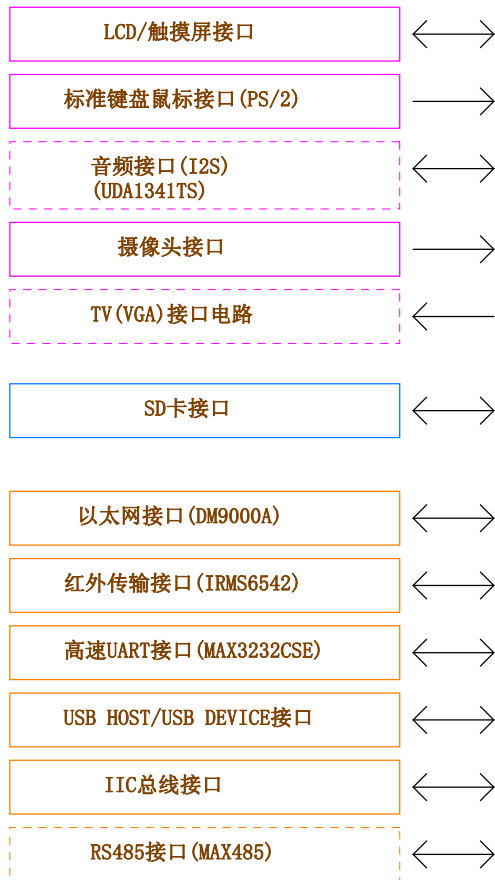
ZHI CHEN TECH  
南京利瑪電子

Organization = 南京工程学院 通信工程系  
Address = 南京市江宁科学园弘景大道1号  
Phone Code = 025-86113857  
Postal Code = 211167

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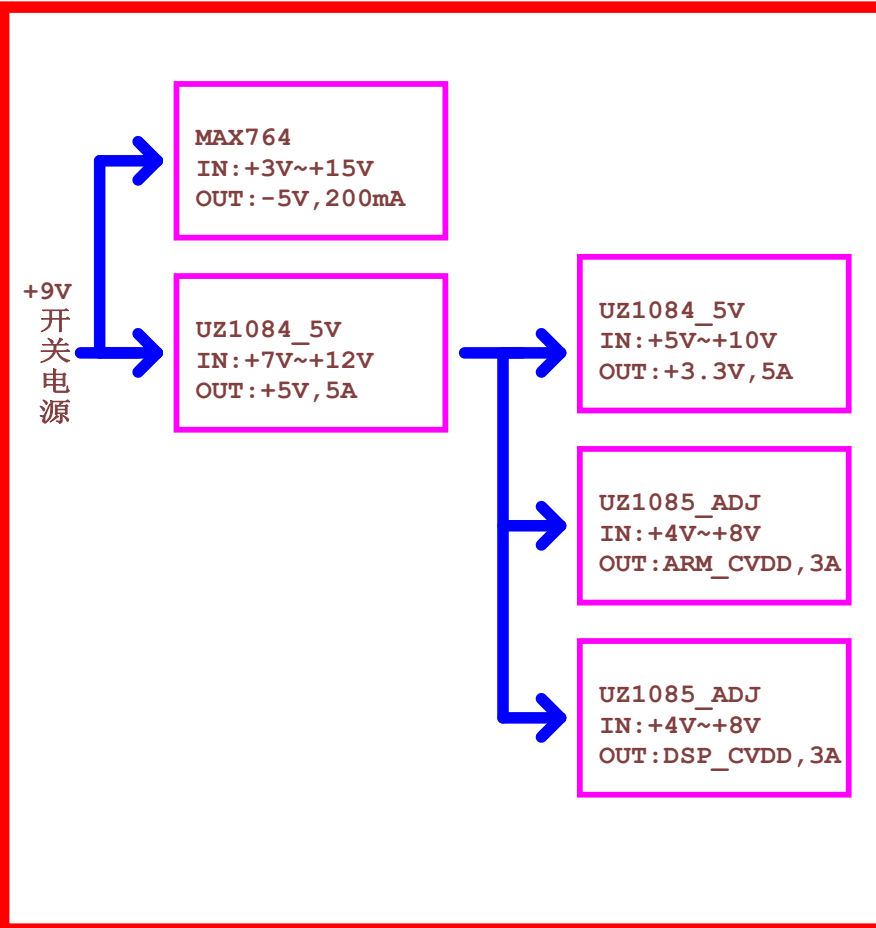




电源方案:

主要器件电流、功耗:

Device	Voltage					Power	Notes
	ARM_CVDD	DSP_CVDD	+3.3V	-5V	+5V		
S3C2440A			26.26mA			368mW	
TMS320C6713BGDP225/300		945mA	75mA				
HY57V561620FTP X 4			180mA			1W	
K9F1208U0M			30mA				
SST39VF1601			35mA (W)				
EPM240T100			25mA				
MAX1420ECM			78+8mA			258mW	
MAX5884EGM			27+8+5.5mA			134mW	
CS4272			53mA			510mW	
DM9000A			92mA				
MAX3232CSE X 2			1mA			696mW (70°C)	
Sum							



D

C

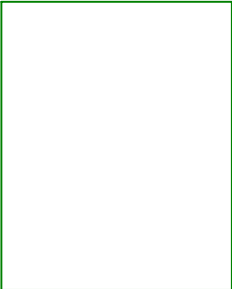
B

A

01ARM  
ARM



02DSP  
DSP

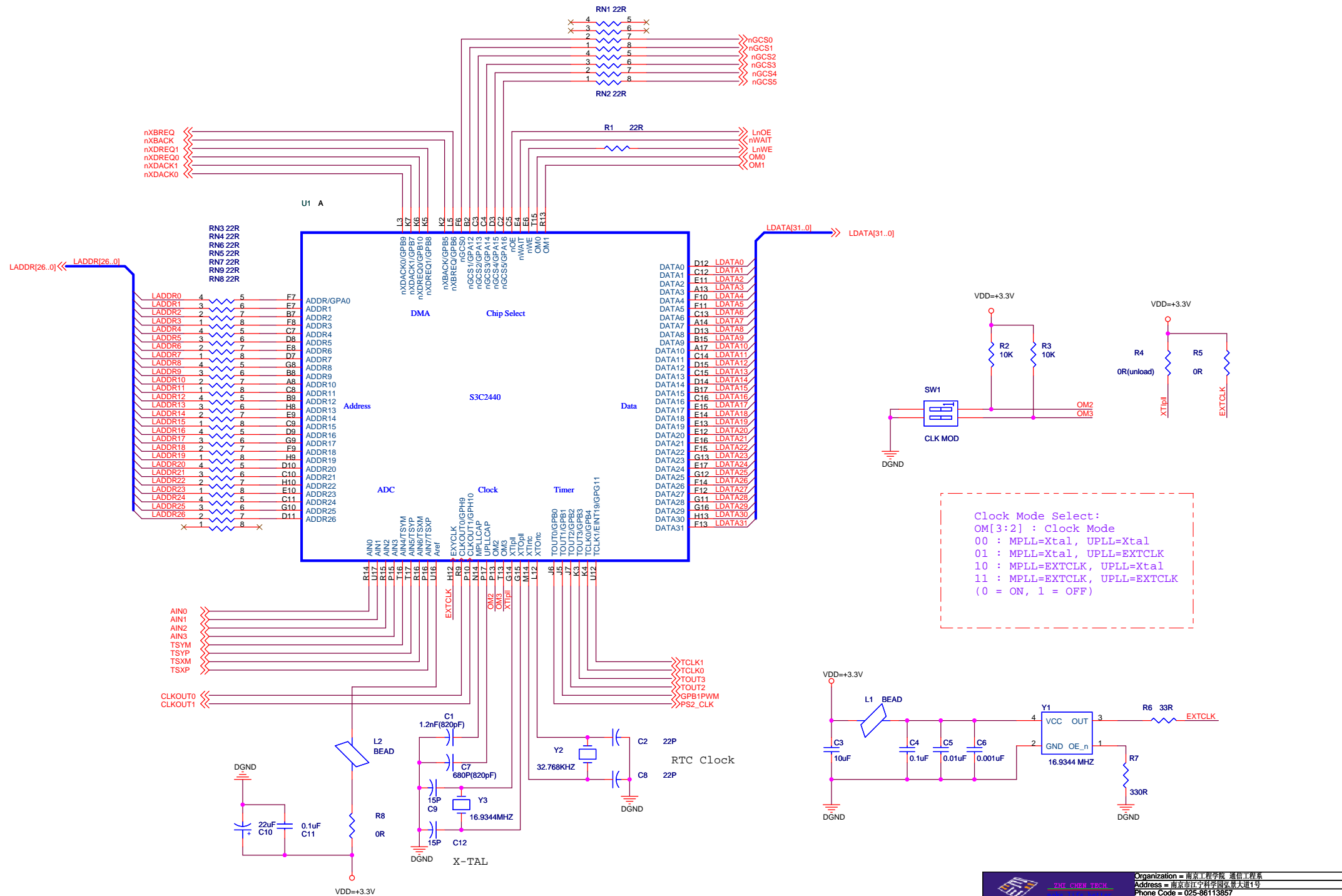


03POWER  
POWER

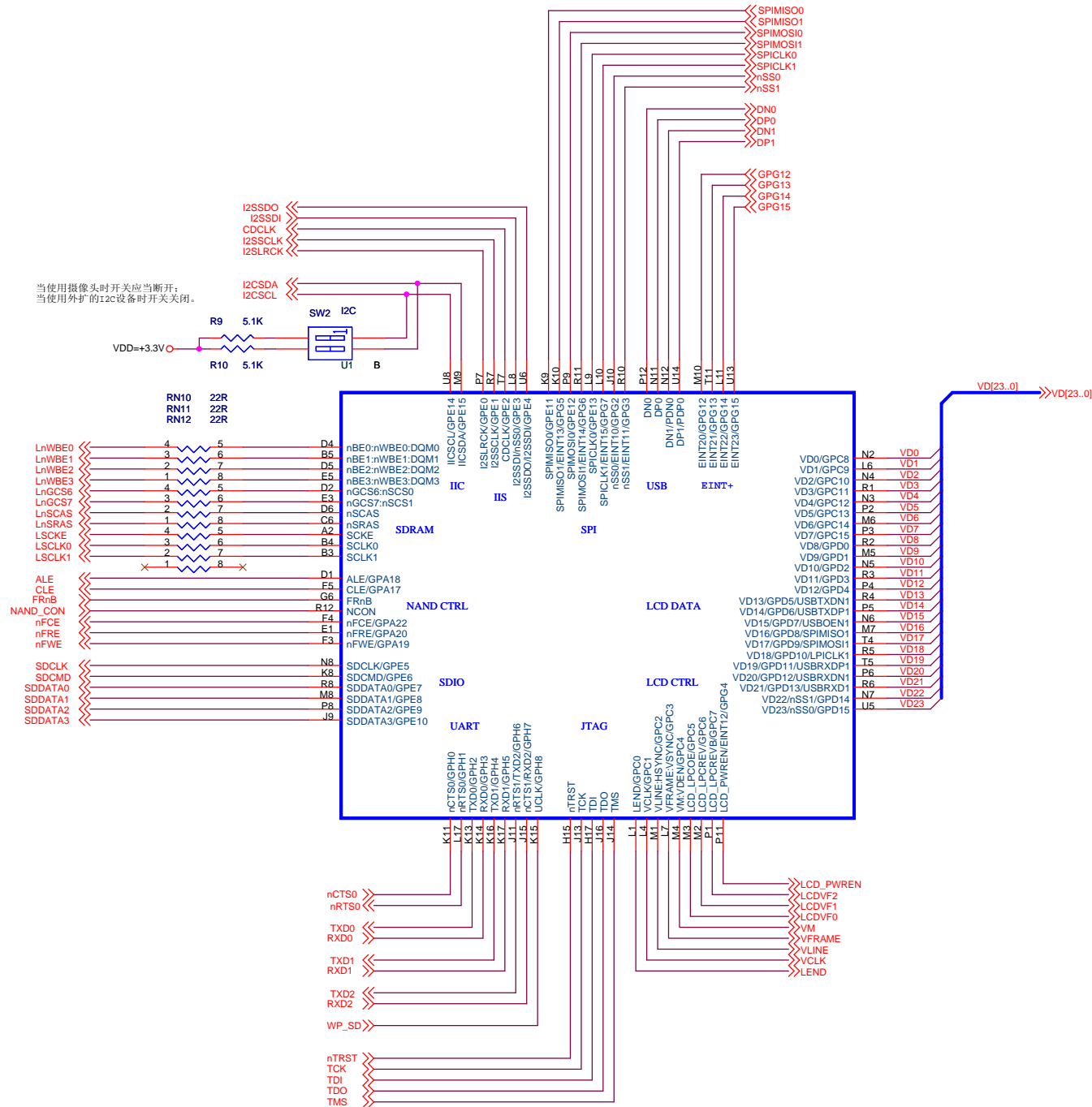


DSP和ARM接口：  
DSP                      ARM

HASn	VCC
HDS1n	nOE
HDS2n	nWE
HCSn	nGCS1
HRDYn	nWAIT
HINT	EINT8
HCNT0	ADDR2
HCNT1	ADDR3
HR/Wn	ADDR4
HHWIL	ADDR1



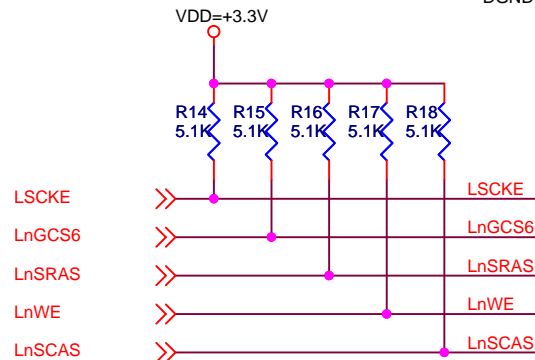
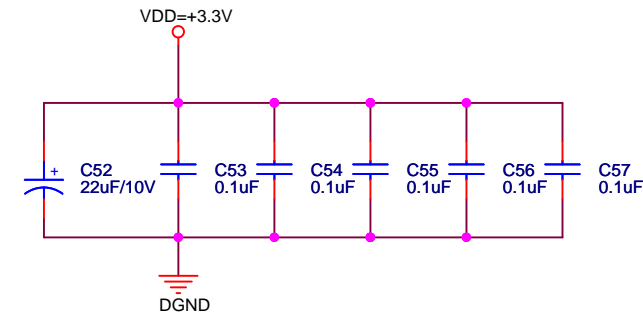
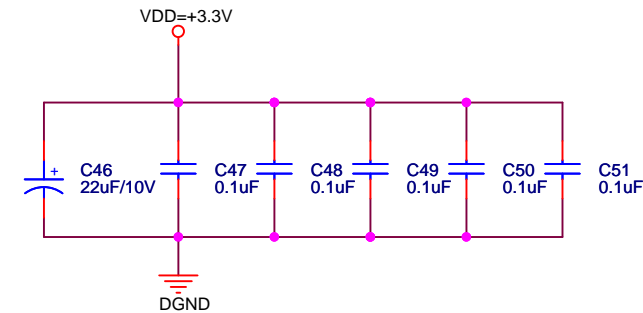
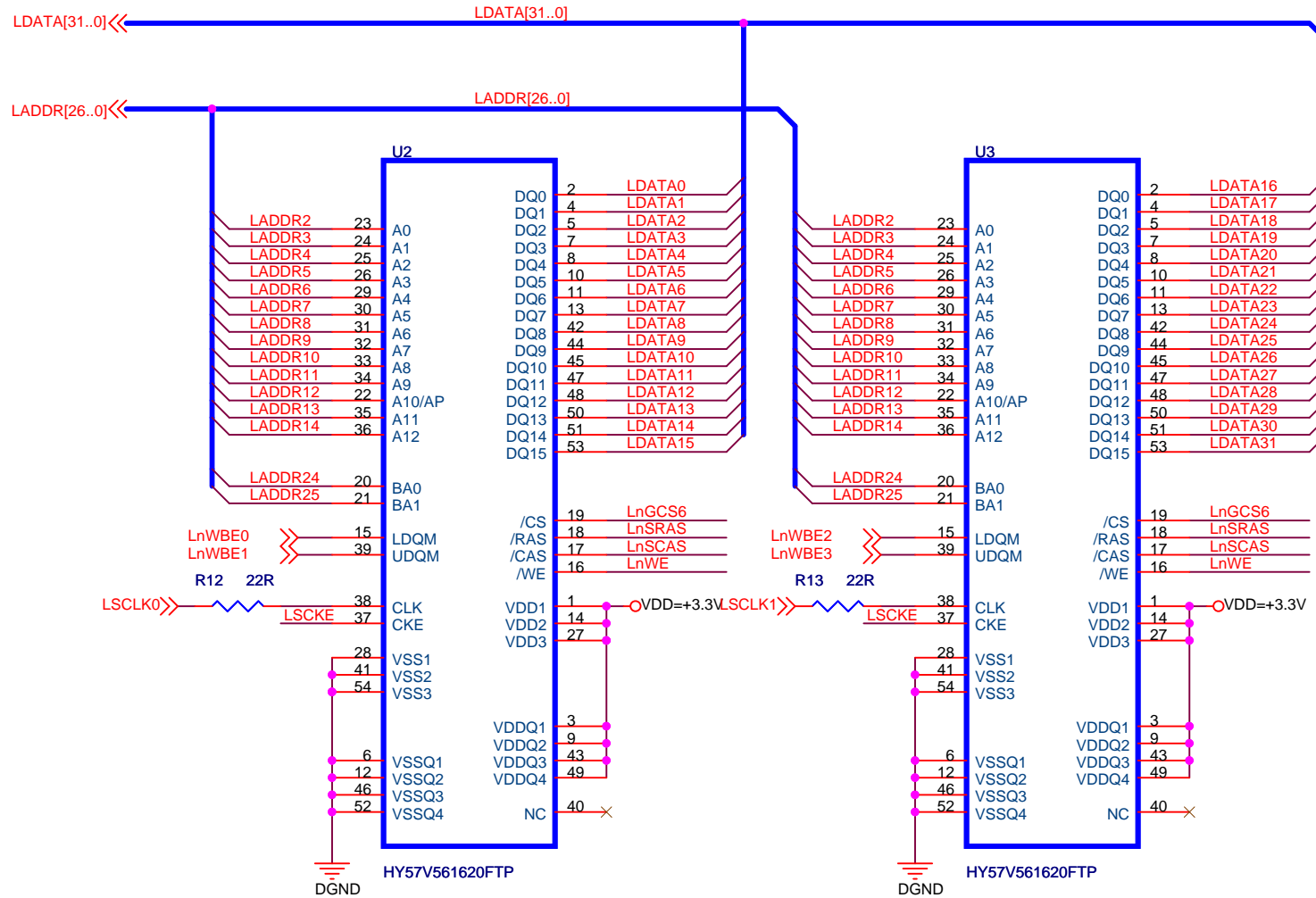
Clock Mode Select:  
OM[3:2] : Clock Mode  
00 : MPLL=Xtal, UPLL=Xtal  
01 : MPLL=Xtal, UPLL=EXTCLK  
10 : MPLL=EXTCLK, UPLL=Xtal  
11 : MPLL=EXTCLK, UPLL=EXTCLK  
(0 = ON, 1 = OFF)






低位

高位

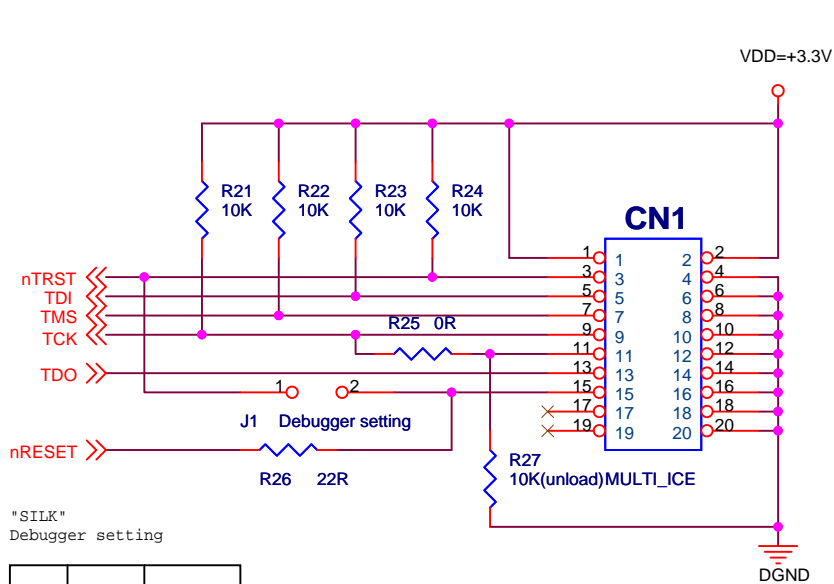


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	Organization = 南京工程学院 通信工程系		
	Address = 南京市江宁科学园弘景大道1号		
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	Postal Code = 211167		
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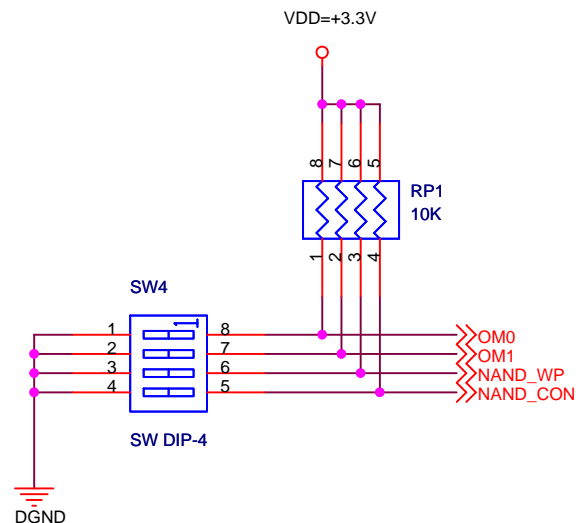




"SILK"  
Debugger setting

	Use	No use
J?	Open	Short

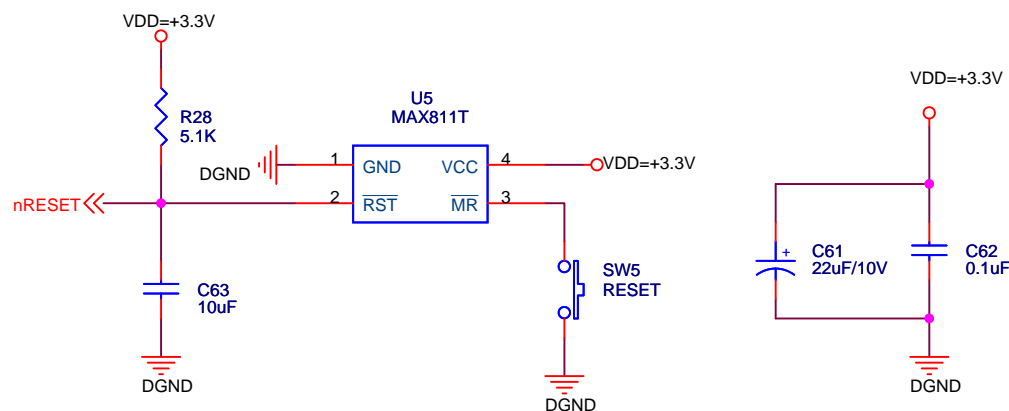
JTAG/Multi-ICE Connect



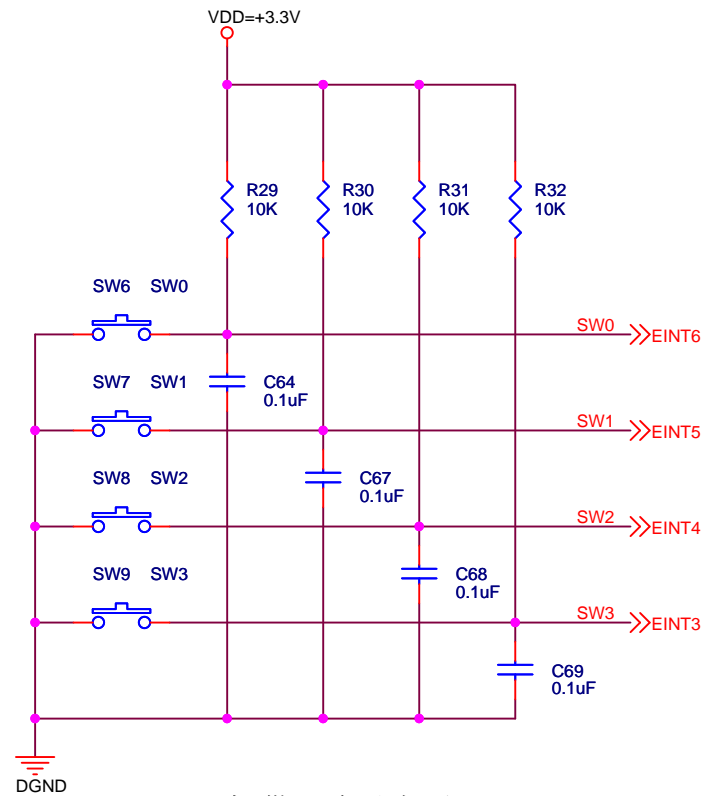
OM[1:0] : Bus Size  
00 : Nand boot  
01 : Halfword (16-bit)  
10 : Word (32-bit)  
11 : Test Mode

/WP:  
NAND Flash write protect  
NCON:  
NAND Flash Configuration

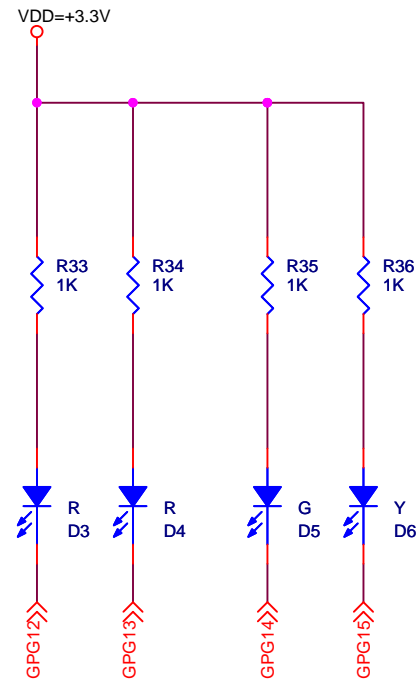
Boot Select



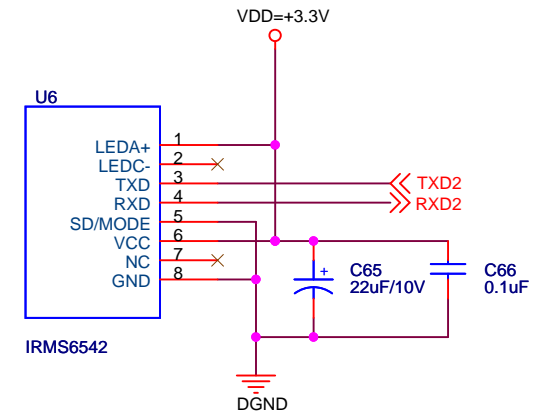
RESET




提供下降沿电平

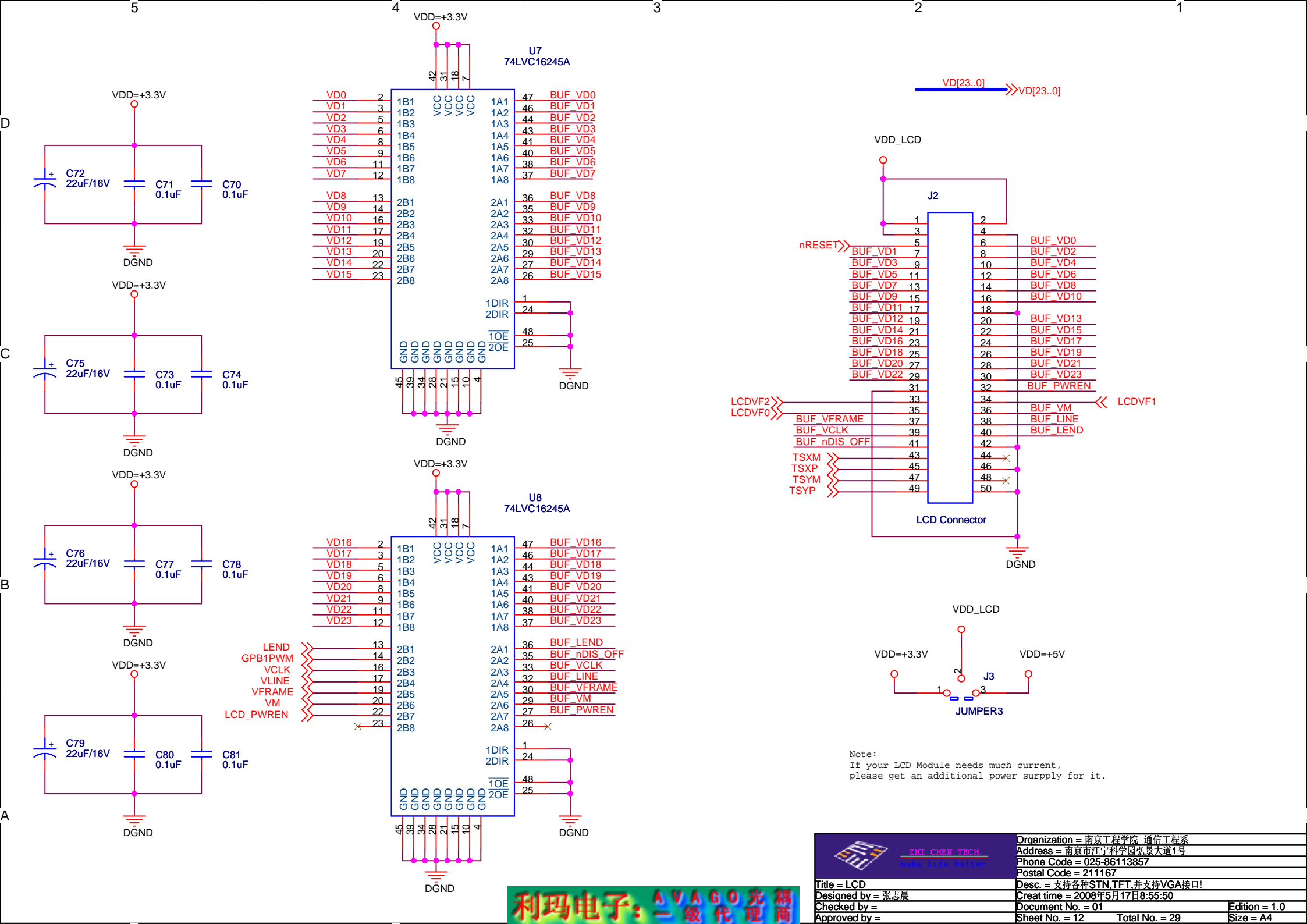


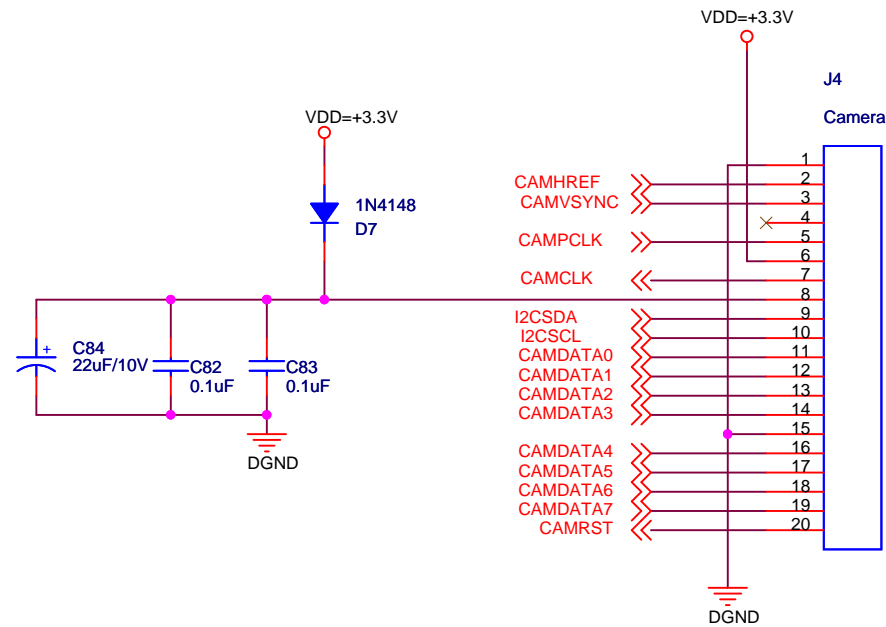
发光二极管




一体化红外发射接收头

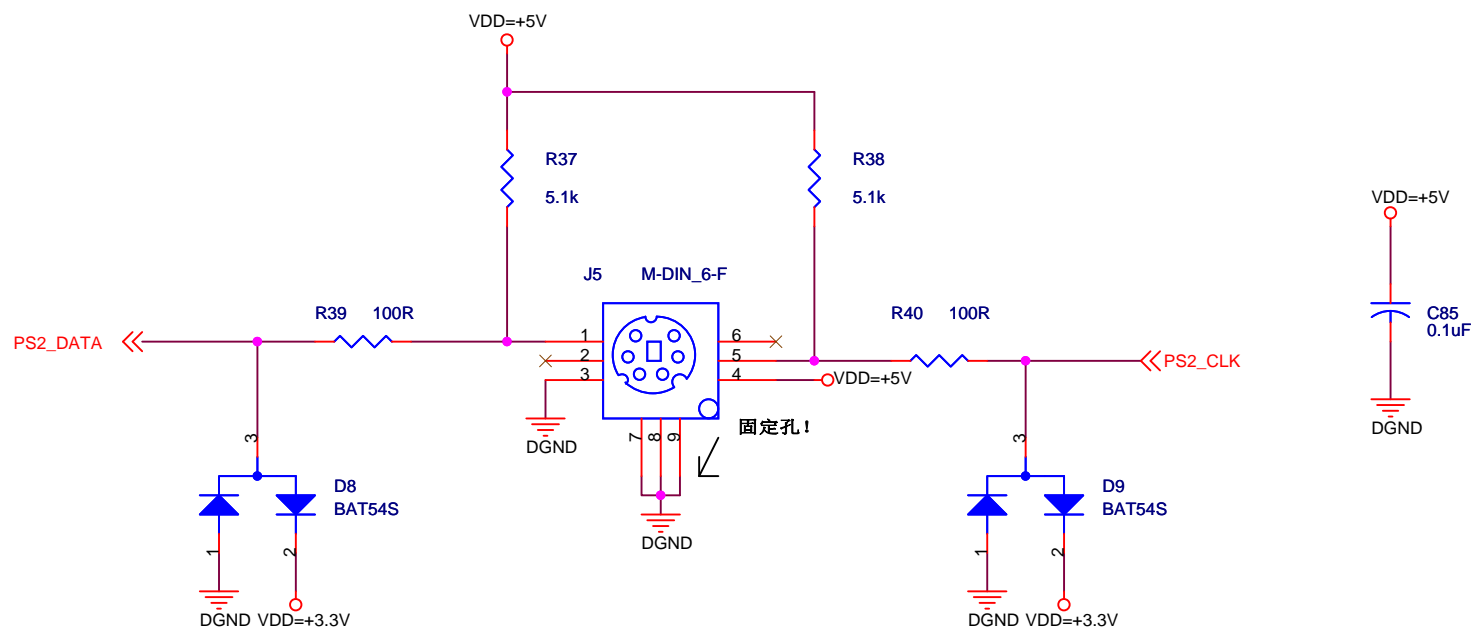
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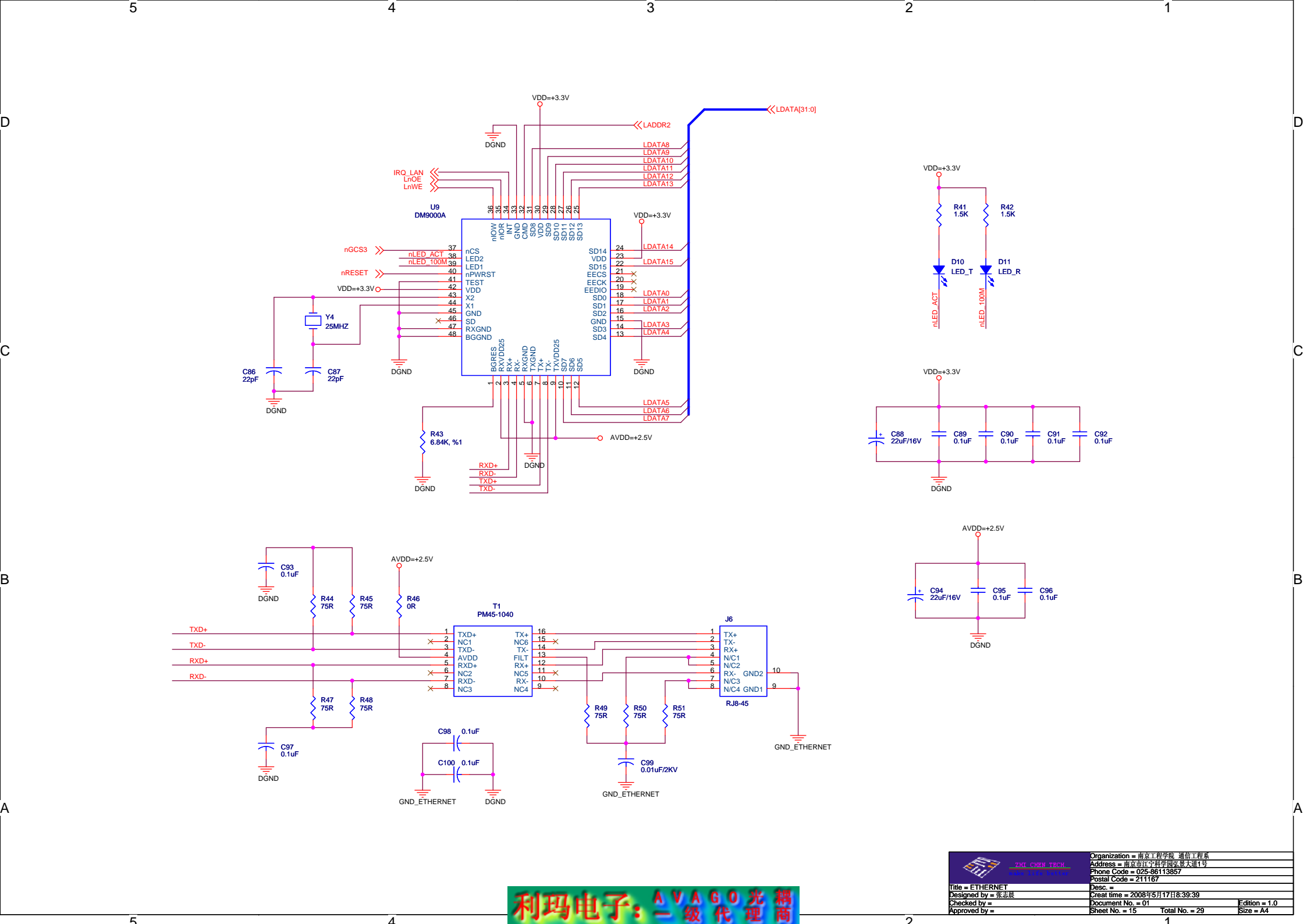
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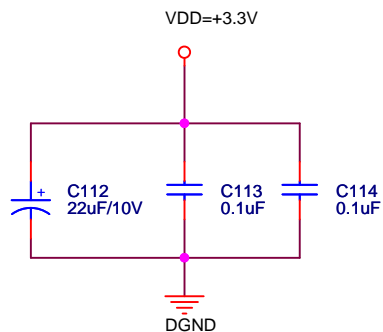
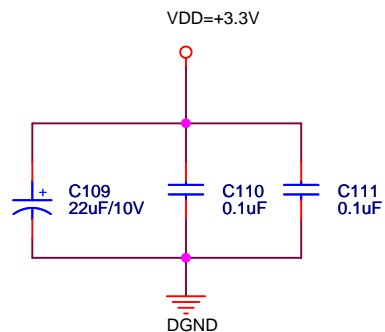
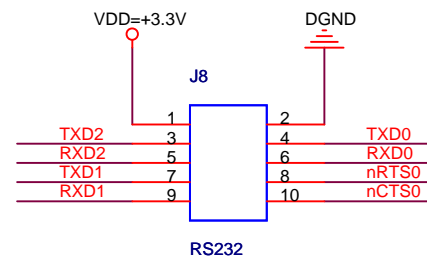
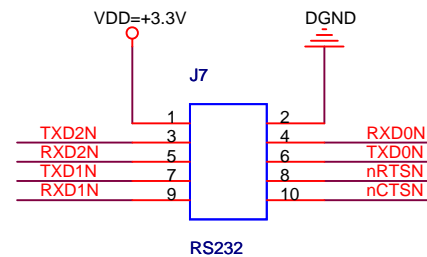
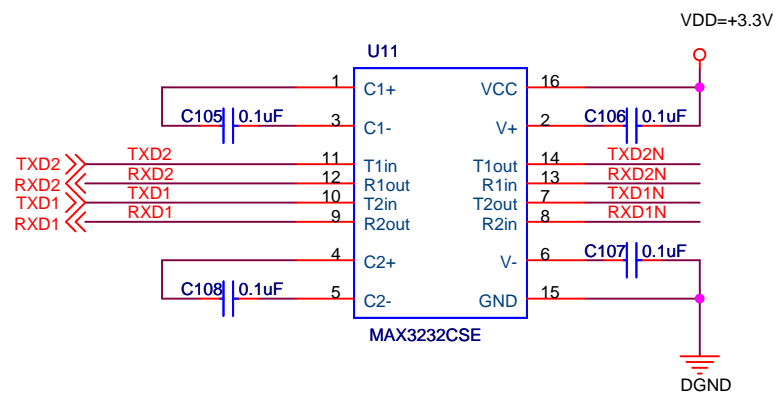
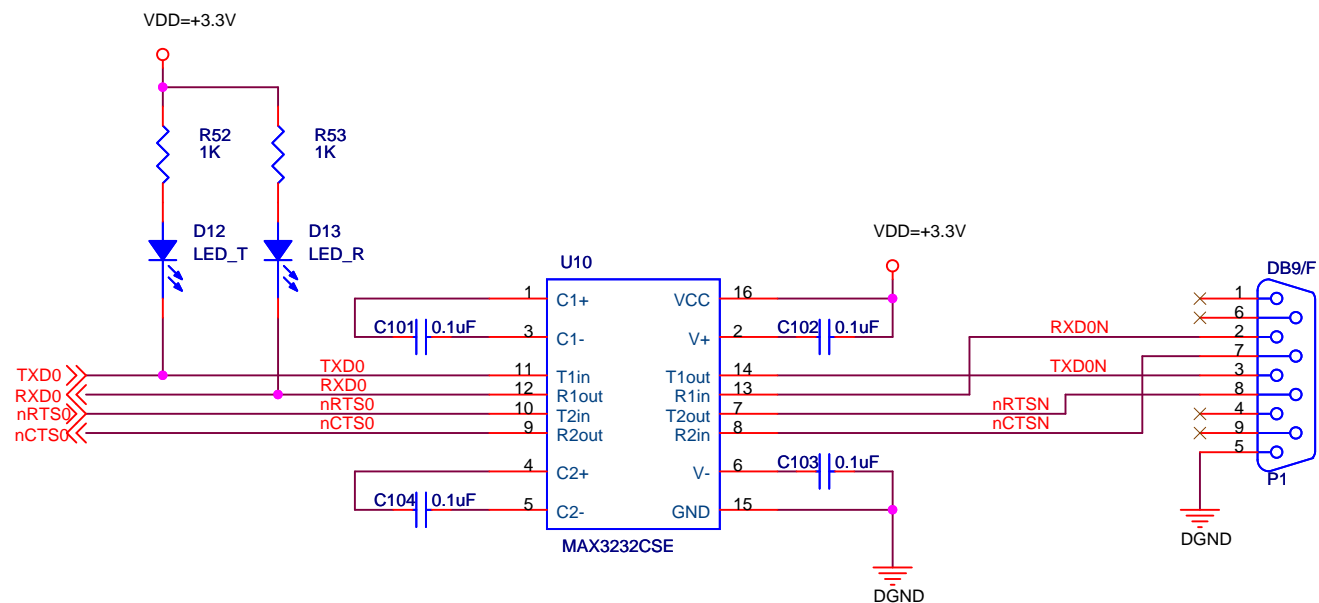
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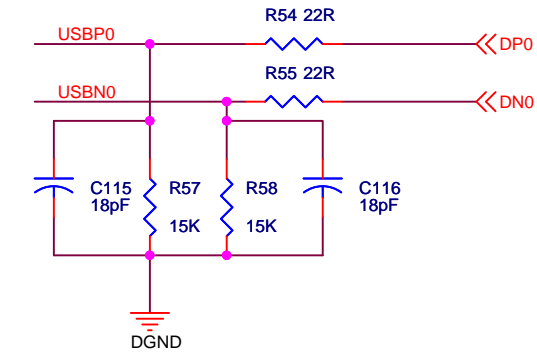
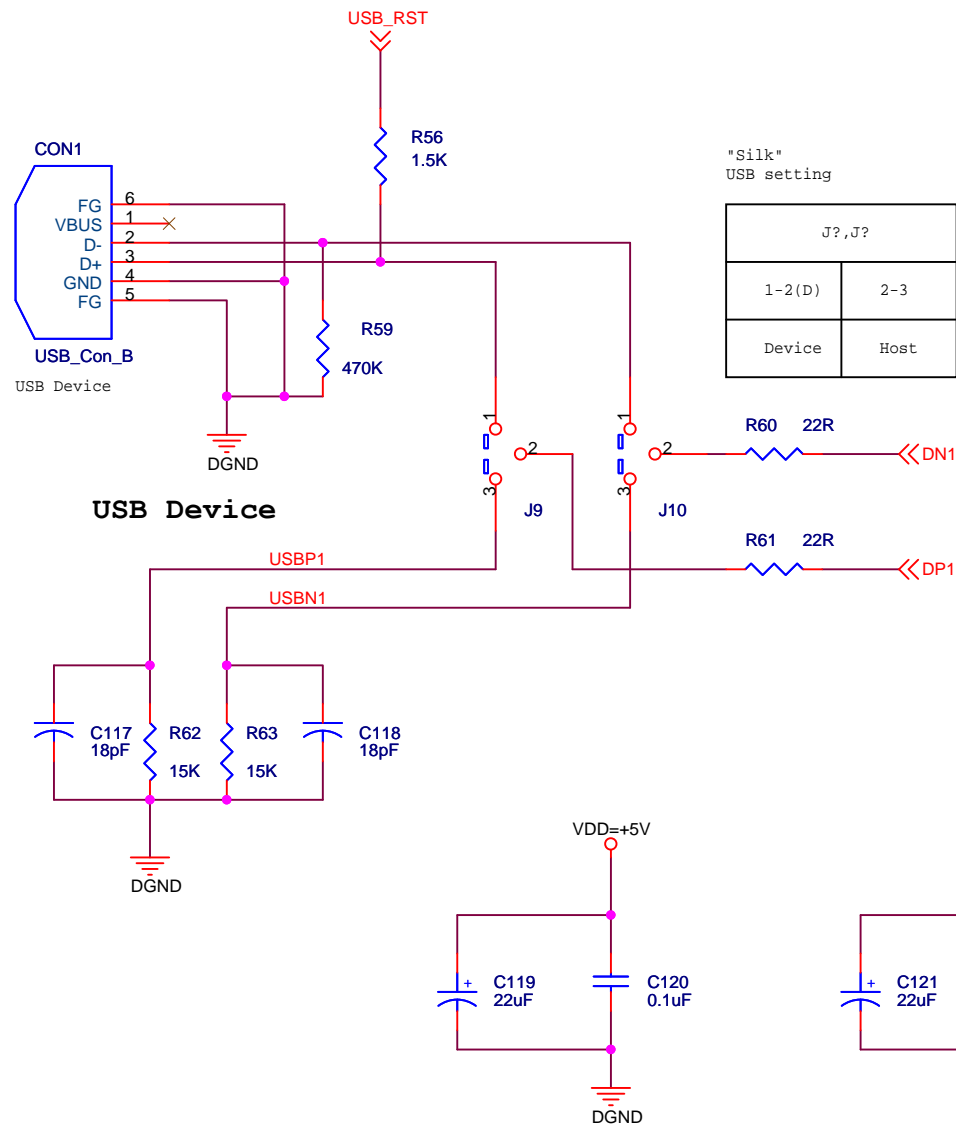
Male	Female	6-pin Mini-DIN (PS/2):	6 脚 Mini-DIN(PS/2)
		1 - Data	1—数据
		2 - Not Implemented	2—未实现，保留
		3 - Ground	3—电源地
		4 - +5v	4—电源+5V
(Plug) 插头	(Socket) 插座	5 - Clock	5—时钟
		6 - Not Implemented	6—未实现，保留

注明：一般鼠标、键盘上为Male，PC主板接口为Female。

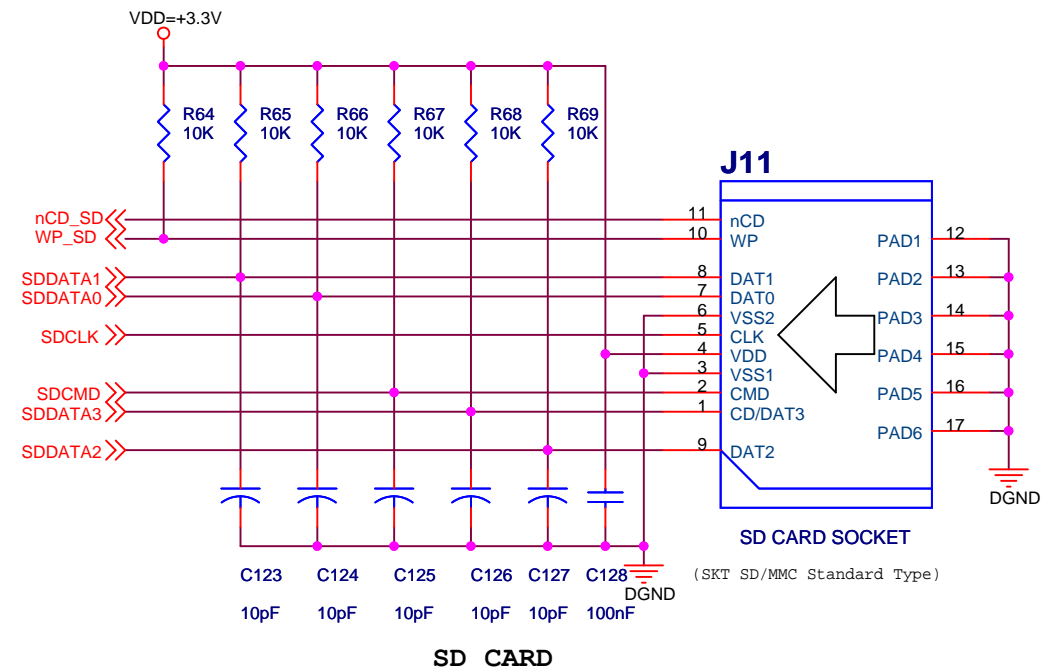


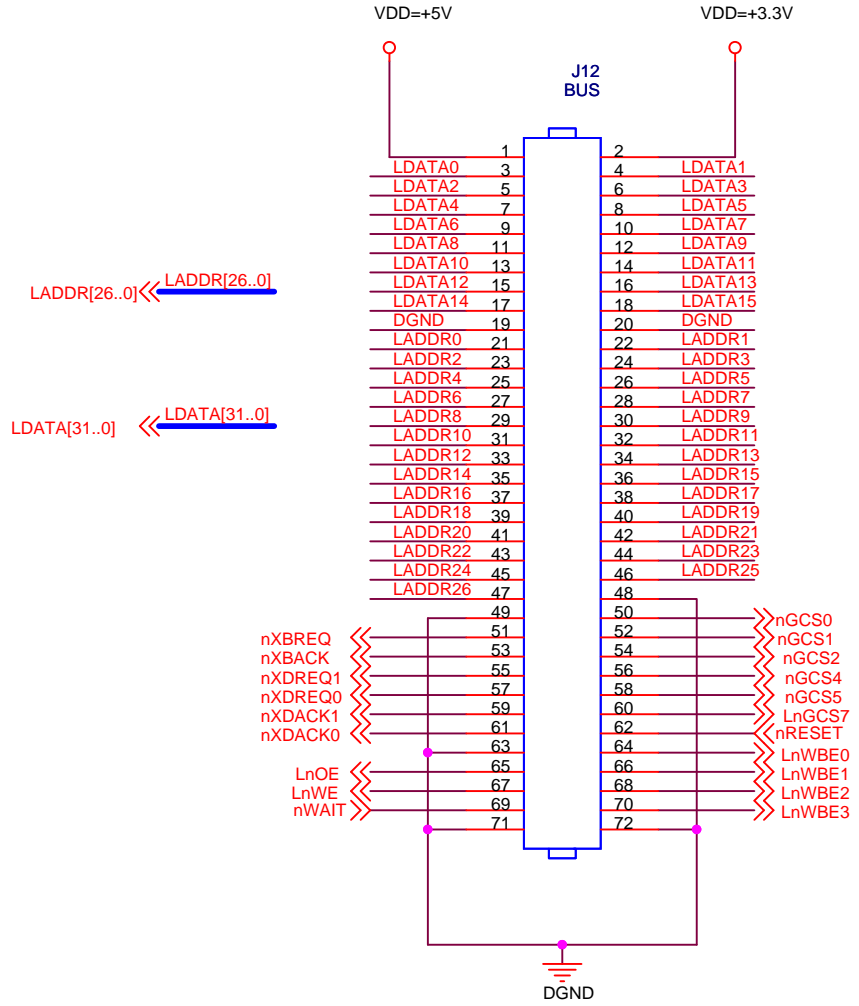






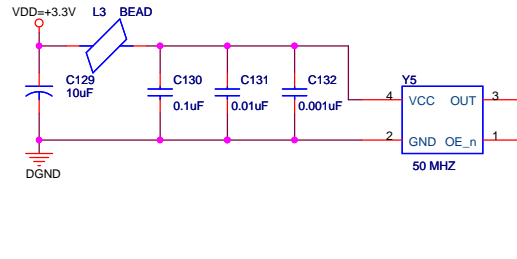
USB Host





Clock output at half of device speed (O/Z) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] pin (I/O/Z)

Clock output programmable by OSCDIV1 register in the PLL controller.



Device Endian Mode (HD8)

0 - Big Endian  
1 - Little Endian

Big Endian Mode Correctness EMIFBE (HD12)

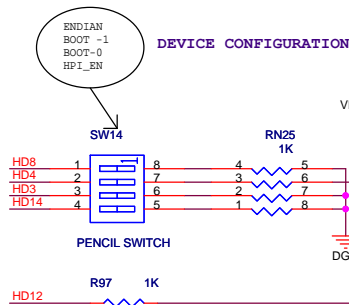
0 - The EMIF data will always be presented on the ED[7:0] side of the bus, regardless of the endianness mode (Little/Big Endian).  
1 - In Little Endian mode (HD8 = 1), the 8-bit or 16-bit EMIF data will be present on the ED[7:0] side of the bus.

Bootmode (HD[4:3])

00 - HPI boot/Emulation boot  
01 - CE1 width 8-bit, Asynchronous external ROM boot with default timings (default mode)  
10 - CE1 width 16-bit, Asynchronous external ROM boot with default timings  
11 - CE1 width 32-bit, Asynchronous external ROM boot with default timings

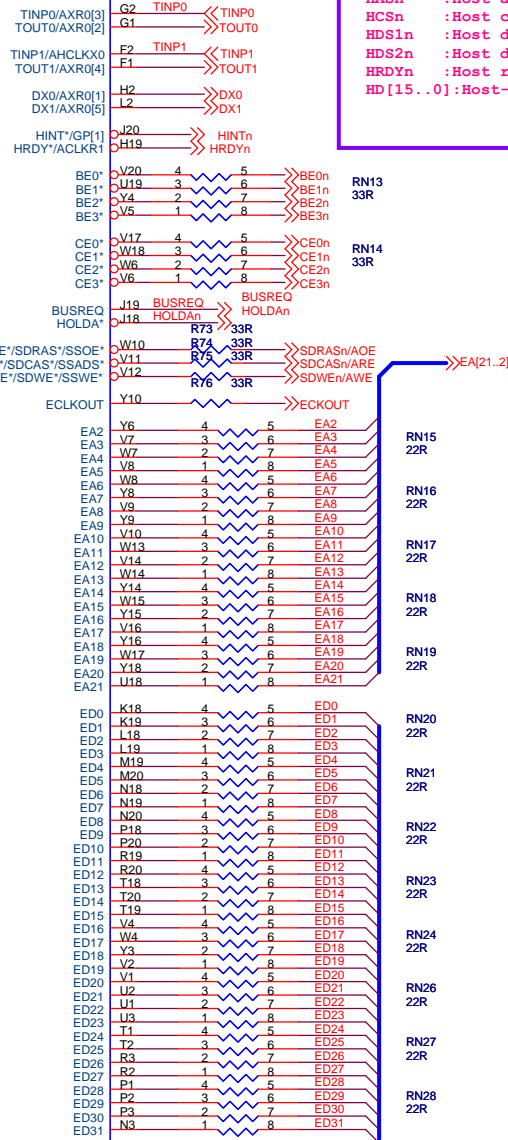
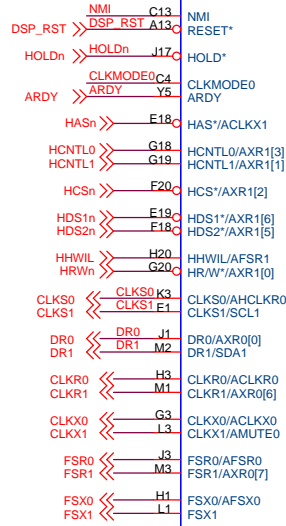
HPI\_EN (HD14)

0 -HPI disabled, McASPI enabled  
1 -HPI enabled, McASPI disabled (default)



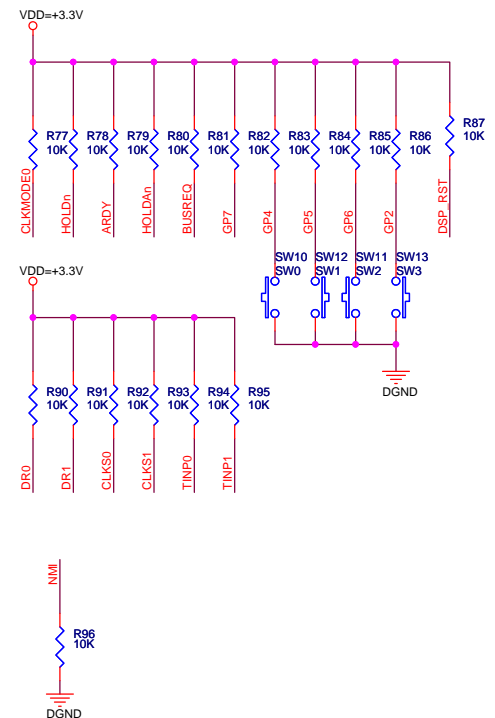
General-purpose input/output pins (I/O/Z) which also function as external interrupts!

U12  
TMS320C6713BGP225 A



#### HPI接口说明:

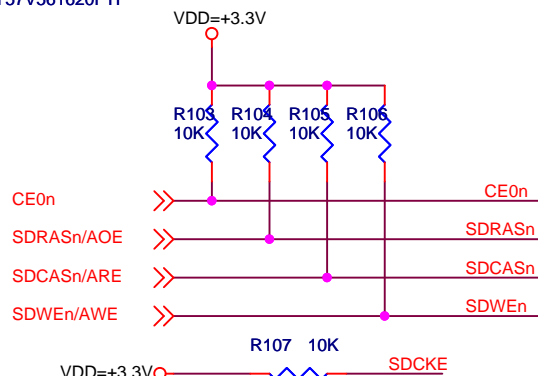
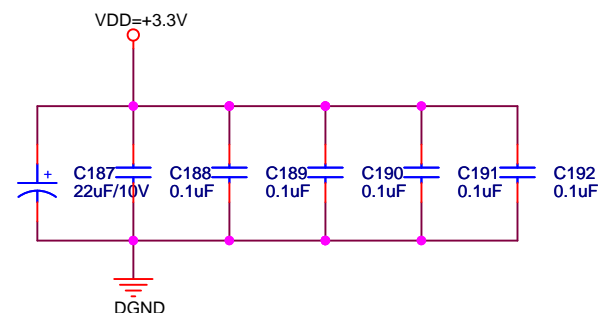
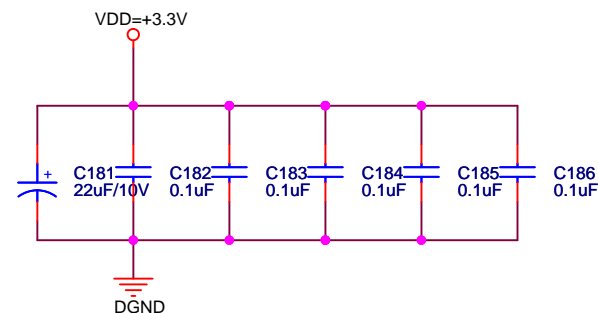
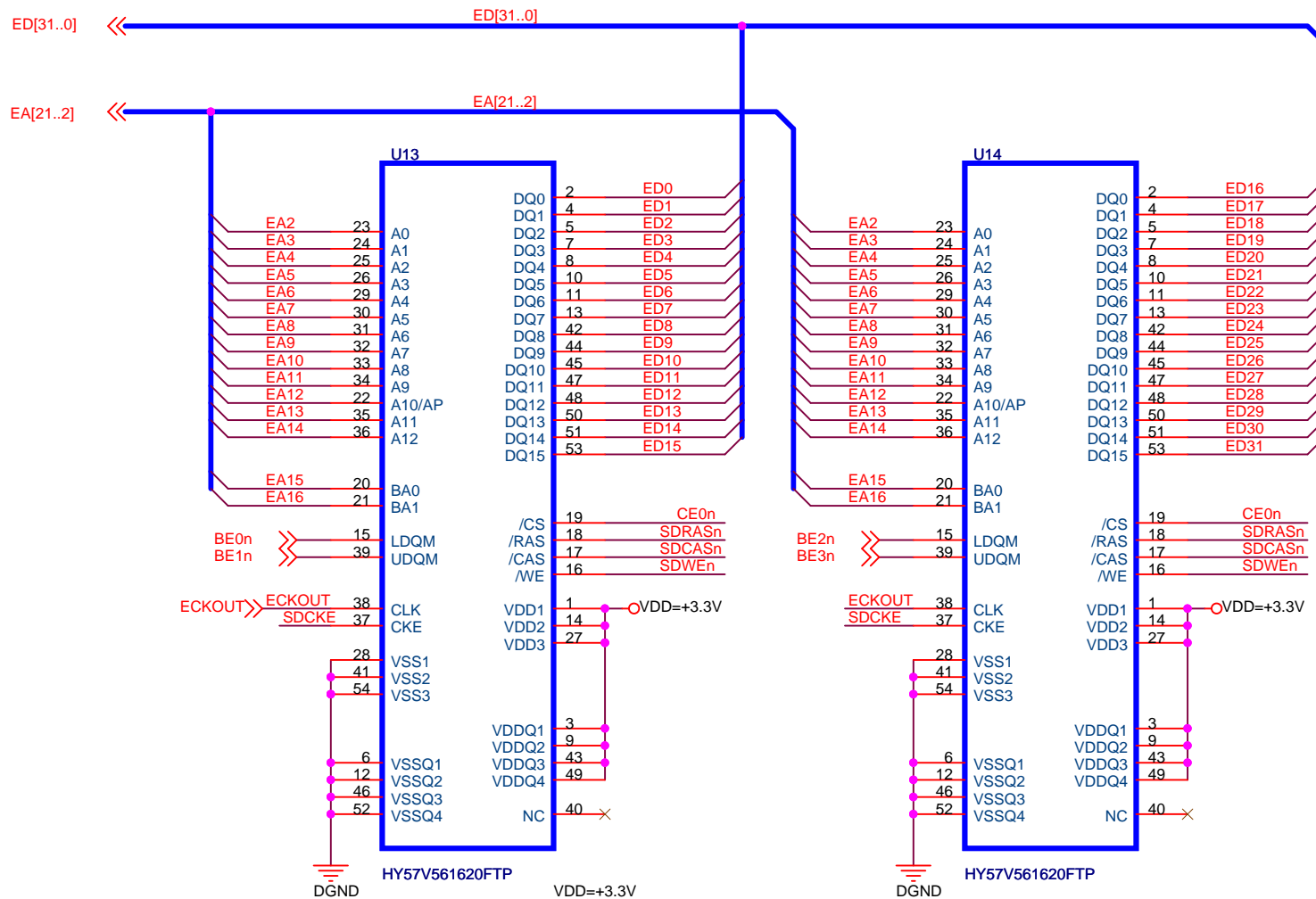
HINTn :Host interrupt (from DSP to host)  
HCNTL0 :Host control - selects between control, address, or data registers  
HCNTL1 :Host control - selects between control, address, or data registers  
HHWIL :Host half-word select - first or second half-word  
HRWn :Host read or write select  
HASn :Host address strobe  
HCSn :Host chip select  
HDS1n :Host data strobe 1  
HDS2n :Host data strobe 2  
HRDYn :Host ready (from DSP to host)  
HD[15..0]:Host-port data pins



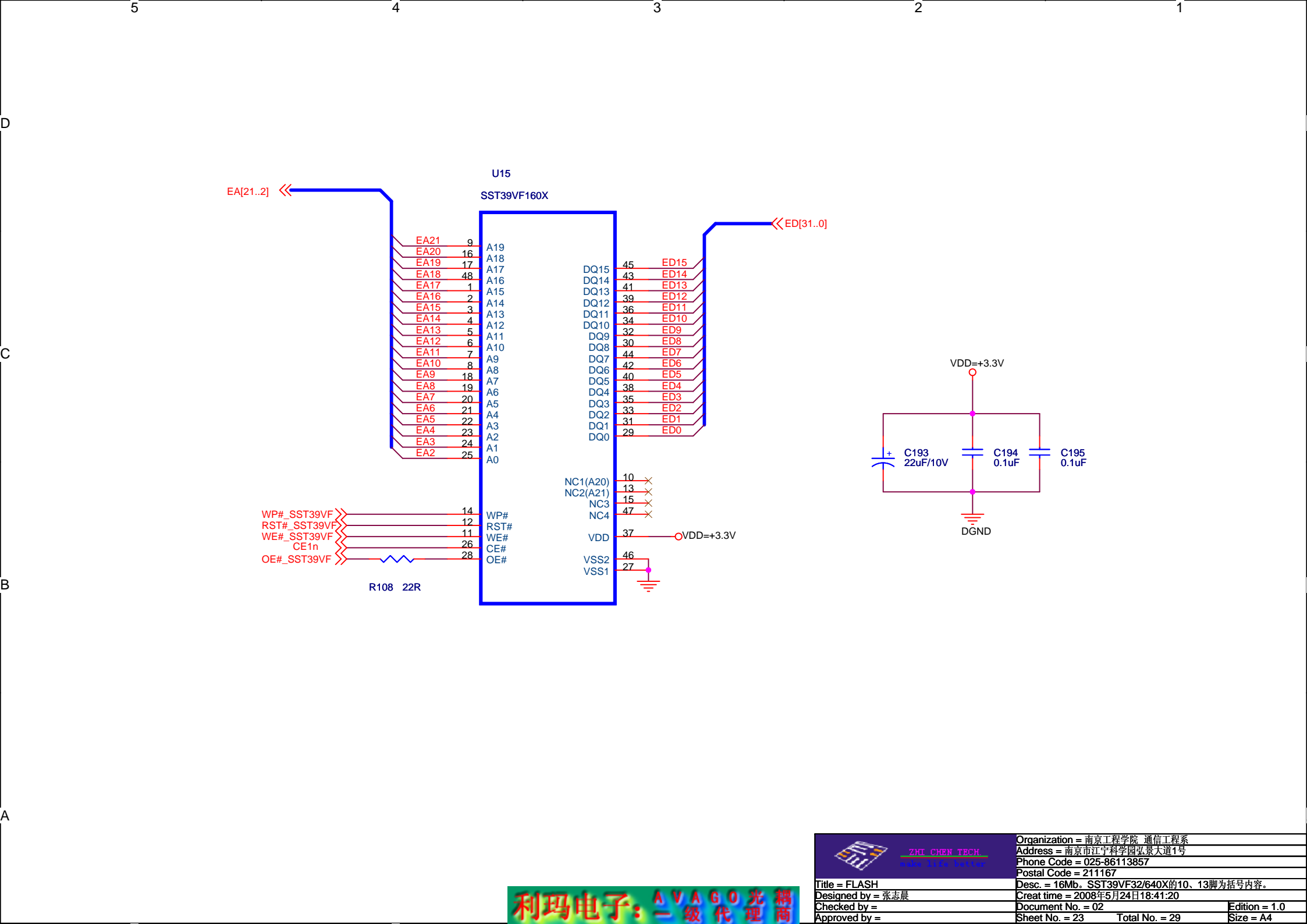


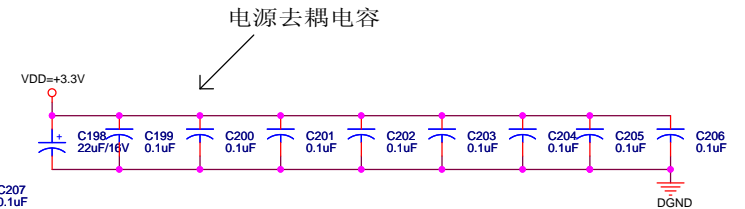
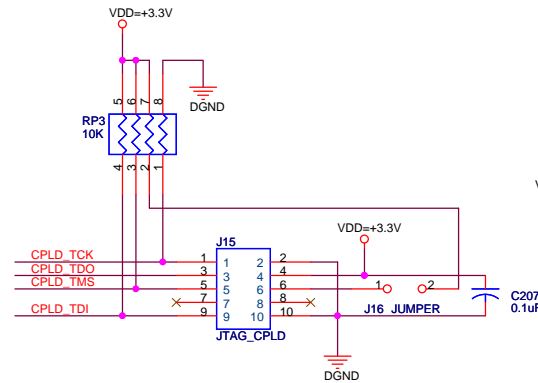
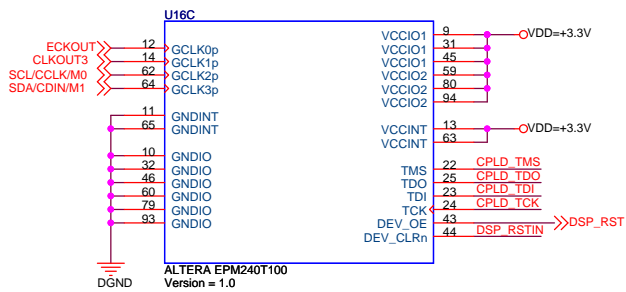
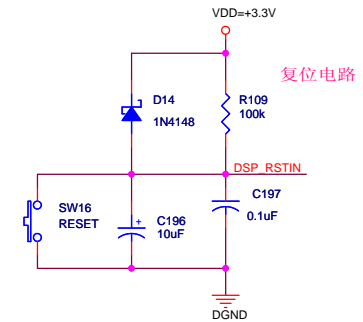
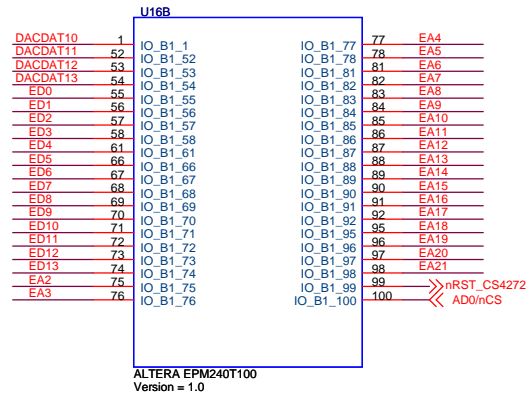
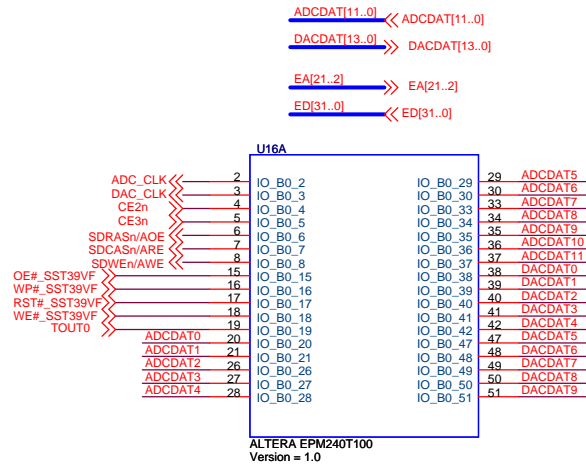
低位

高位



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Notes:

"1. For EPM240 devices, all VCCINT pins must be connected to either 3.3 V or 2.5 V, but not a combination of both."

" For EPM240G devices, all VCCINT pins must be connected to 1.8 V."

"2. Each set of VCCIO pins (VCCIO1 or VCCIO2) can be connected to 3.3 V, 2.5 V, 1.8 V, or 1.5 V."



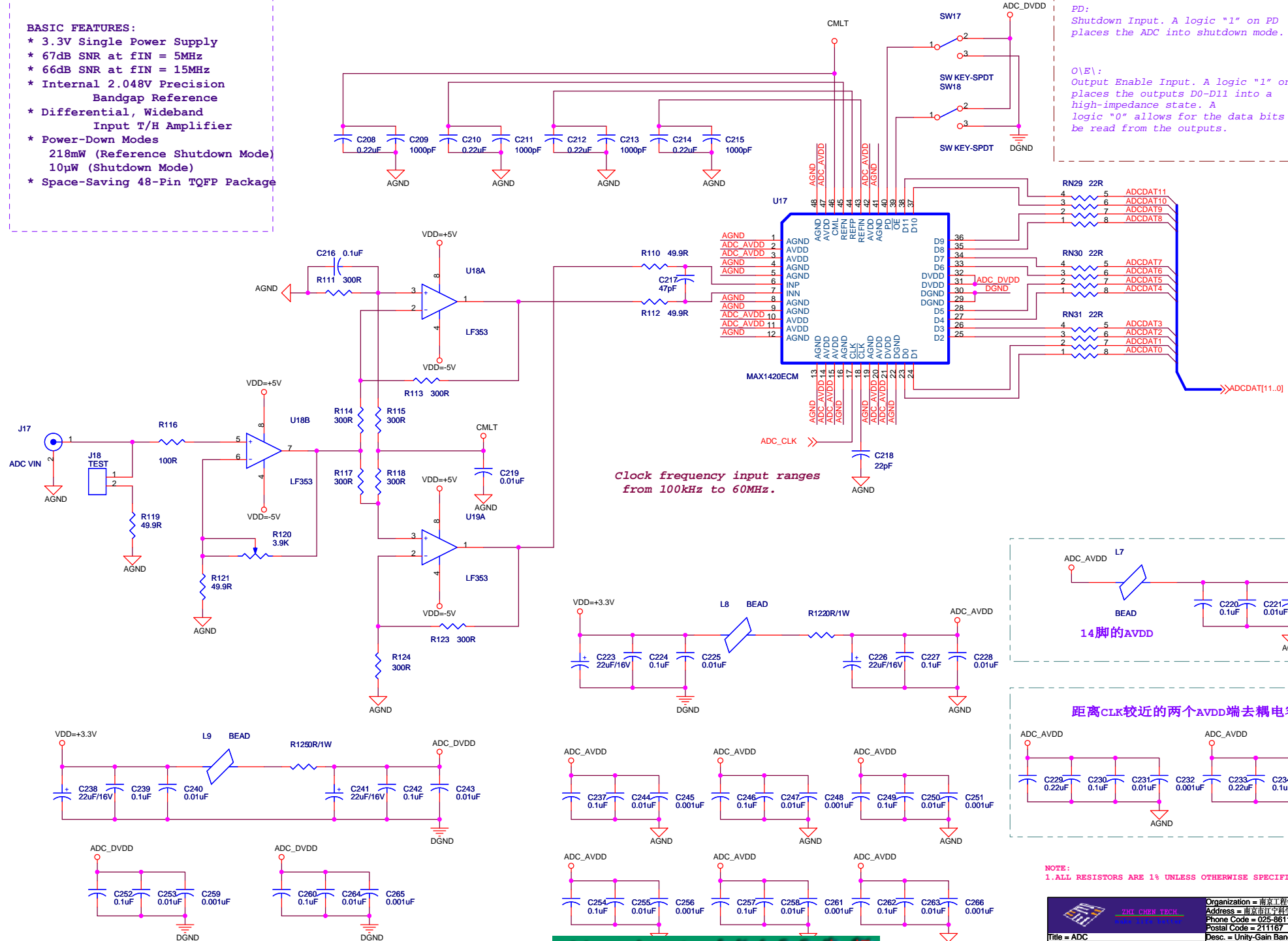
### BASIC FEATURES:

- \* 3.3V Single Power Supply
- \* 67dB SNR at  $f_{IN} = 5\text{MHz}$
- \* 66dB SNR at  $f_{IN} = 15\text{MHz}$
- \* Internal 2.048V Precision Bandgap Reference
- \* Differential, Wideband Input T/H Amplifier
- \* Power-Down Modes
  - 218mW (Reference Shutdown Mode)
  - 10 $\mu$ W (Shutdown Mode)
- \* Space-Saving 48-Pin TQFP Package

一般情况下这两个管脚都接地。

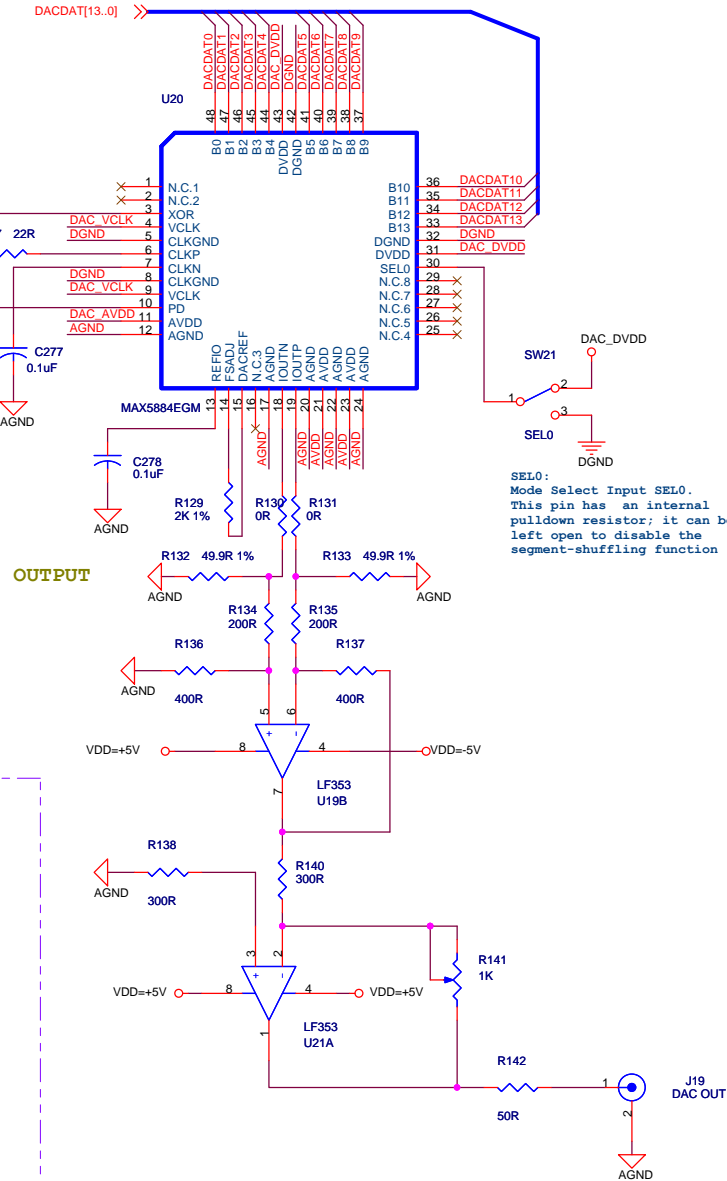
PD:  
Shutdown Input. A logic "1" on PD places the ADC into shutdown mode.

O/E\:  
Output Enable Input. A logic "1" on OE places the outputs D0-D11 into a high-impedance state. A logic "0" allows for the data bits to be read from the outputs.



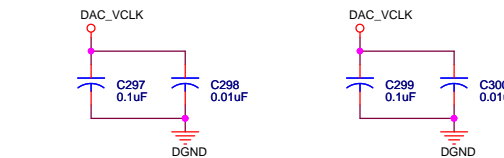
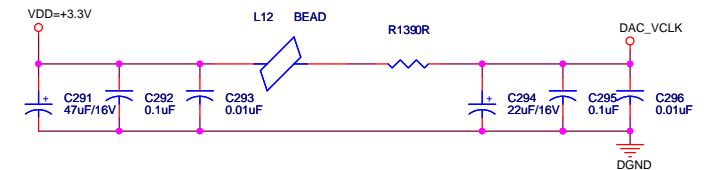
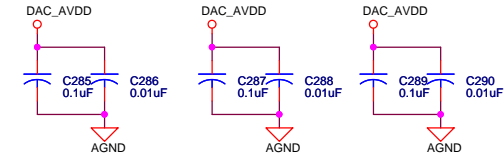
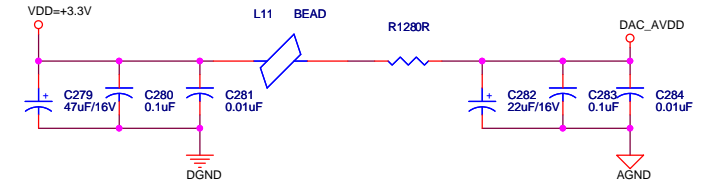
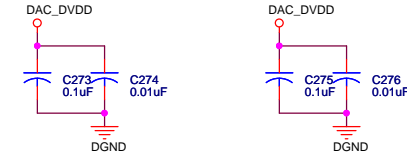
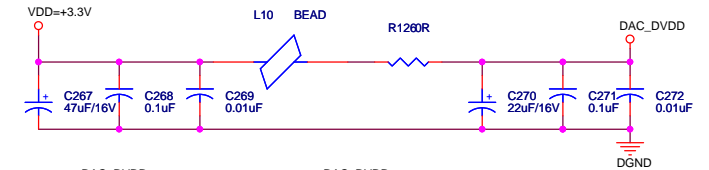
XOR:  
XOR Input Pin.  
XOR = 1 inverts the digital input data.  
XOR = 0 leaves the digital input data unchanged.  
XOR has an internal pulldown resistor  
and may be left unconnected if not used.

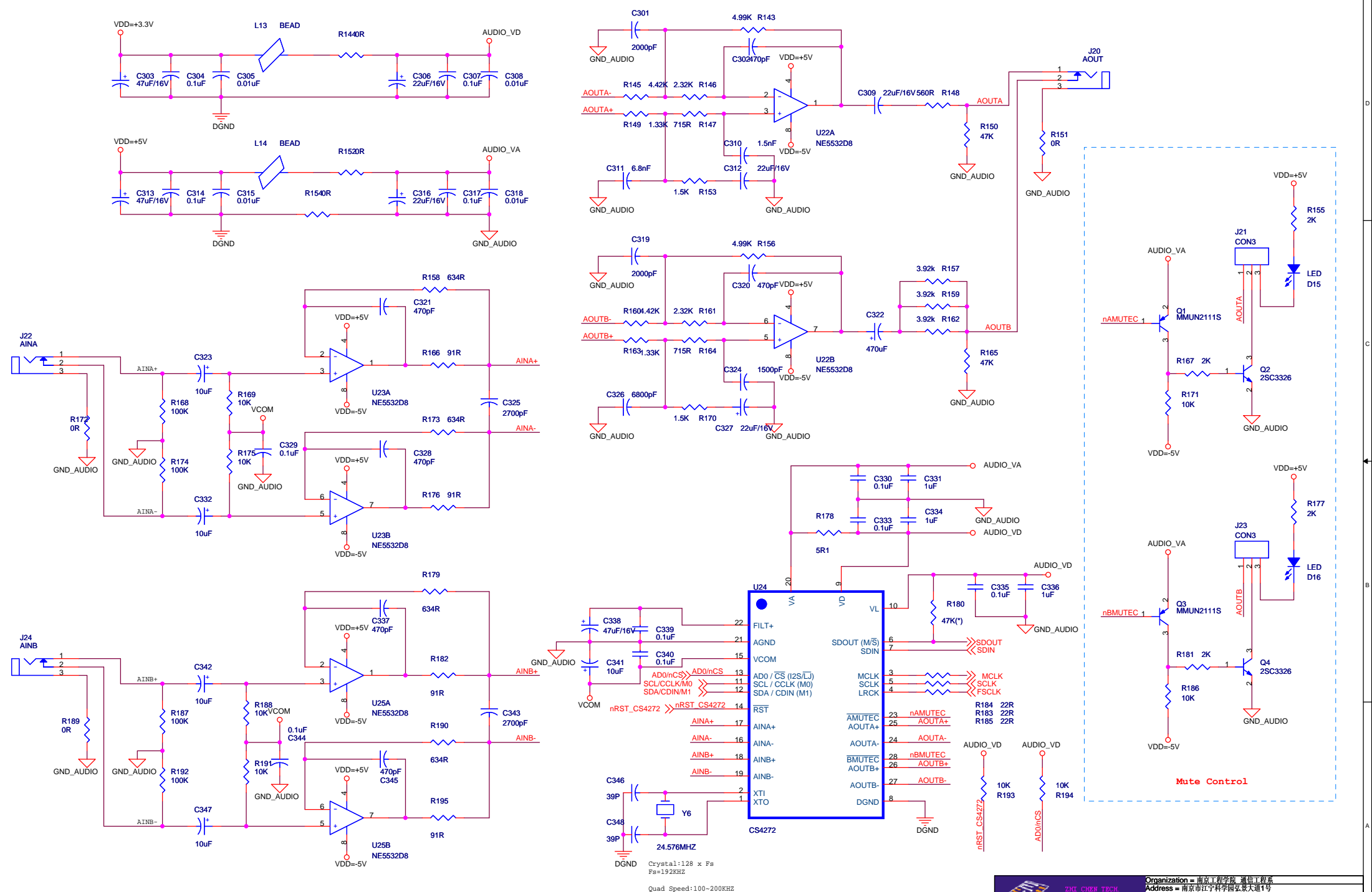
PD:  
Power-Down Input. PD pulled high  
enables the DAC's power-down  
mode. PD pulled low allows  
for normal operation of the DAC.



#### BASIC FEATURES:

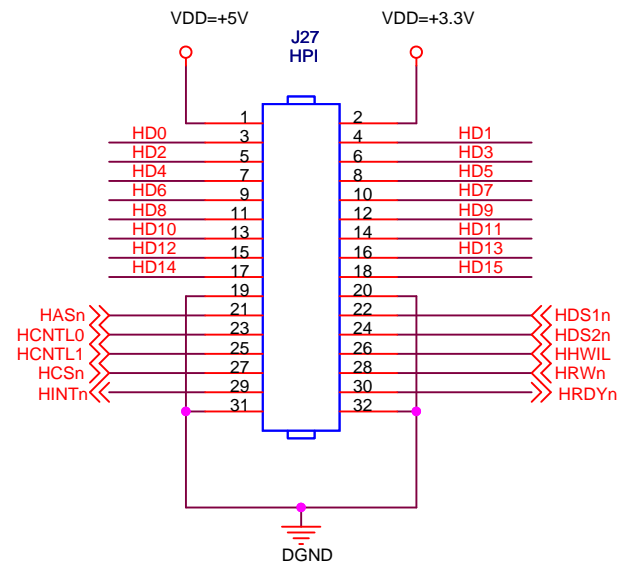
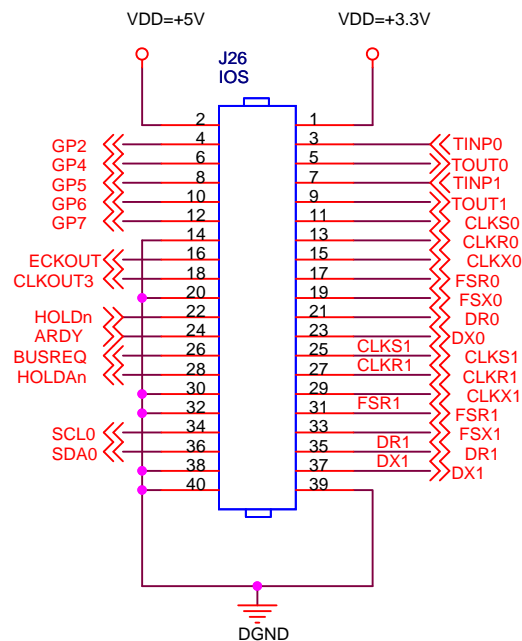
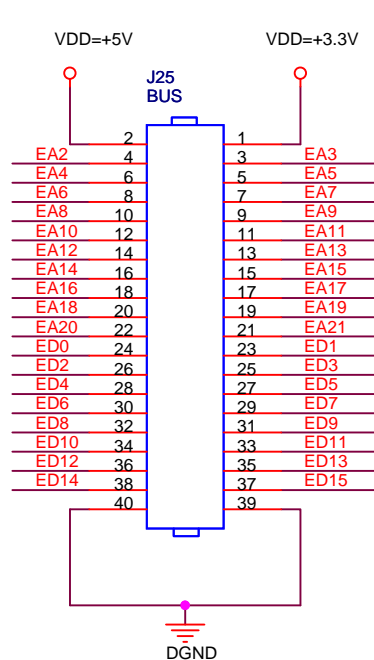
- \* 200Mps Output Update Rate
- \* Single 3.3V Supply Operation
- \* Excellent SFDR and IMD Performance  
SFDR = 77dBc at  $f_{OUT} = 10\text{MHz}$  (to Nyquist)  
IMD = -86dBc at  $f_{OUT} = 10\text{MHz}$   
ACLR = 72dB at  $f_{OUT} = 30.72\text{MHz}$
- \* 2mA to 20mA Full-Scale Output Current
- \* CMOS-Compatible Digital and Clock Inputs
- \* On-Chip 1.2V Bandgap Reference
- \* Low Power Dissipation
- \* 48-Pin QFN-EP Package



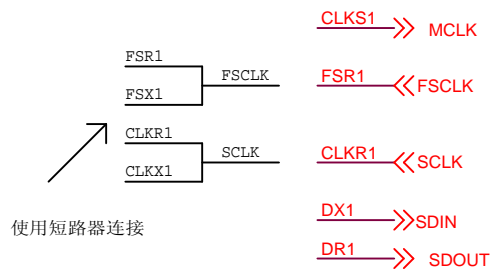


利玛电子: AVAGO 光耦  
一级代理商

ZHI CHEN TECH		Organization = 南京工程学院 通信工程系	
		Address = 南京市江宁科学园弘阳大道1号	
		Phone Code = 025-86113857	
		Postal Code = 211167	
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		Edition = 1.0	
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ED[31..0] << ED[31..0]  
EA[21..2] >> EA[21..2]



AUDIO之McBSP接口

HD[15..0] << HD[15..0]

此为可调式输出连接方式，若要固定输出-5V电压，REF和FB短接，FB和OUT断开即可！

外部为+9V或+12V开关电源输入，由于多数为线性电源芯片，最好为+9V，且电源要能够提供足够的电流！

机械安装孔，接地！

光学基准点，顶层、底层各3个

注：仅在第1.0版中保存这些电压检测点，调试正常后，将会去掉！